REMARKS

Claims 55-78, and 85-89 remain in this application. No claims have been added,

cancelled, or amended. The Applicants respectfully request reconsideration of this

application in view of the above amendments and the following remarks.

35 U.S.C. §103(a) Rejection - Gates in view of Carlsson

The Examiner has rejected claims 55-78 and 85-89 under 35 U.S.C. §103(a) as

being obvious over U.S. Patent No. 5,701,409 issued to Gates (hereinafter referred to as

"Gates") in view of U.S. Patent No. 4,053,947 issued to Carlsson et al. (hereinafter

"Carlsson"). The Applicants respectfully submit that the present claims are allowable

over any combination of Gates and Carlsson.

Claim 75 recites a method comprising at least, "detecting a bug of the component

by determining an incorrect response of the component to the predefined sequence of bus

These limitations are not taught by any combination of Gates and transactions".

Carlsson.

Gates does not teach or suggest detecting a bug of the component by determining

an incorrect response to the predefined sequence of bus transactions. A concise summary

of the approach discussed in <u>Gates</u> is provided in the abstract:

"In order to test a parallel digital bus, an integrated circuit adapted for coupling

to the bus has a bus error generation circuit which generates and/or simulates

bus error conditions on the bus. During test, an error command is loaded into a

command register of the bus error generation circuit via the bus. The bus error

generation circuit then decodes the command, and either: 1) generates an error

condition on the bus during a subsequent bus cycle, or 2) simulates an error

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condition on the bus during a subsequent bus cycle. A status configuration

register in the integrated circuit and status configuration registers in other

devices on the bus are then read to determine whether the integrated circuit and

other devices properly detected and/or handled the generated or simulated error.

By providing a bus error generation circuit in the integrated circuits coupled to a

bus inside personal computer, built-in test of the personal computer is facilitated"

Accordingly, Gates discusses using a single error command to generate or

simulate an error on a bus. As understood by the Applicants, the error command is a

"dedicated" error command that generates or simulates an error by forcing the bus error

generation circuit to invert a parity bit. As stated in Gates, "[a]fter a particular error

command is loaded into the command register ... the bus error generation circuit causes

an incorrect parity value to be output onto the PCI bus terminal PAR during a

subsequent data write PCI bus cycle" (column 2, lines 49-53). A specific example of this

is discussed at column 4, lines 37-42.

Now, the error command of Gates literally is not a predefined sequence of bus

transactions. The Office Action appears to admit this when it acknowledges that Gates

fails to teach storing more than one command.

Referring now to the other reference, Carlsson also does not teach or suggest

detecting bugs, let alone detecting bugs by determining an incorrect response to a

predefined sequence of bus transactions. Accordingly, any combination of Gates and

<u>Carlsson</u> does not teach or suggest the claims limitations.

The Examiner has taken Official Notice with regards to the storing of multiple

commands in an instruction memory for the purpose of speeding up the time needed to

process instructions. In response, the Applicants respectfully submit that this is not well

known in the context of the claims to store a plurality of instructions representing a

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predefined sequence of bus transactions in the instruction memory for purposes of

detecting a bug of the component by determining an incorrect response of the component

to the predefined sequence of bus transactions. If the Examiner intends for the Official

Notice to encompass anything more than the statement that multiple instructions may be

stored in a memory, then it is respectfully requested that the Examiner state more

precisely what the Official Notice encompasses, and provide a reference in support of the

notice, as required by the Rules. The same applies with other Official Notices taken in

the Office Action.

The Examiner went on to state that it would have been obvious, to a person of

ordinary skill in the art at the time the invention was made to use an instruction memory

for multiple instructions, in Gates, to speed up processing. The Applicants respectfully

submit that the Examiner has failed to establish a prima facie case of obviousness.

To establish a prima facie case of obviousness, three basic criteria must be met.

First, there must be some suggestion or motivation, either in the references themselves or

in the knowledge generally available to one of ordinary skill in the art, to modify the

references or to combine reference teachings. Second, there must be a reasonable

expectation of success. Finally, the prior art reference (or references when combined)

must teach or suggest all the claim limitations. The teaching or suggestion to make the

claimed combination and the reasonable expectation of success must both be found in the

prior art, and not based on Applicant's disclosure. In re Vaeck, 947 F.2d 488, 20

USPQ2d 1438 (Fed. Cir. 1991).

Applicants contend that the above Office Action fails to establish a prima facie

case of obviousness for at least the reason that even if Gates is modified, as proposed by

the Examiner, it still does not teach or suggest all claim limitations. Even if Gates were

modified to store multiple instructions in the instruction memory, as proposed by the

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examiner, the multiple instructions would still be the error commands of Gates. As

discussed above, each of the error commands alone generate or simulate an error on a bus

by forcing the bus error generation circuit to invert a parity bit. As understood by

Applicants, there is no provision whatsoever in Gates for determining an incorrect

response to a sequence of multiple error commands. Accordingly, even if Gates were

modified as proposed by the Examiner, it still would not teach or suggest all of the

claimed elements.

The claimed elements are significant, since they may allow, in one embodiment,

detecting a bug that may not be detected by the approach discussed in Gates.

discussed in the patent application at page 7, lines 5-12:

"Components, such as processors and chipsets, coupled to complex buses often

contain bugs that cause them to fail during operation. In the failing scenarios,

the components frequently respond incorrectly to specific bus transaction

sequences, even when the bus transaction sequence is "legal"; in other words,

there is nothing in the bus transaction sequence that should have caused the

component to fail. The process of correcting these bugs requires inducing the

failure under controlled conditions to isolate the bug. Part of this process may

require repeating the bus transaction sequence corresponding to the failure."

In contrast, Gates discusses a different problem, namely "determin[ing] whether

the integrated circuit and other devices properly detected and/or handled the generated

or simulated error". Any further modification of Gates to solve the different and foreign

problem posed in claim 75 would be inappropriate. See e.g., In re Wright, 6 USPQ 2d

1959 (1988).

For at least these reasons, claim 75 is believed to be allowable over any

combination of Gates and Carlsson. Claims 76-78 depend from claim 75 and are

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believed to be allowable therefor, as well as for the recitations independently set forth

therein.

Claim 55 recites at least, "an instruction memory to store a plurality of bus

stimuli instructions that represent a predefined sequence of bus transactions, wherein

each transaction has a plurality of transaction phases". As discussed above, any

combination of Gates and Carlsson does not teach or suggest the predefined sequence of

bus transactions. Accordingly, claim 55 is believed to be allowable. Claims 56-65

depend on claim 55 and are believed to be allowable therefor, as well as for the

recitations independently set forth therein.

Claim 66 recites at least, "a plurality of phase engines coupled between the logic

device and the connector to translate the digital logic into signals and provide the signals

to the bus, the plurality of phase engines including a system phase engine, an arbitration

phase engine, a request phase engine, a snoop/error phase engine, and a data phase

engine, the system phase engine, the arbitration phase engine, and the request phase

engine coupled with the flow portion, the snoop/error phase engine coupled with the

request portion, the data phase engine coupled with the data portion". Any combination

of Gates and Carlsson does not teach or suggest these limitations. Accordingly, claim 66

is believed to be allowable. Claims 67-68 depend on claim 66 and are believed to be

allowable therefor, as well as for the recitations independently set forth therein.

Claim 69 recites at least, "a computer containing a file that is based on an

existing simulation stimulus software and that contains a plurality of bus stimuli

instructions that represent a predefined sequence of bus transactions" and "a transaction

generator ... to receive the file and ...provide a plurality of bus compatible signals to the

bus". Any combination of Gates and Carlsson does not teach or suggest these claim

elements. Accordingly, claim 69 is believed to be allowable. Claims 70-71 depend on

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claim 69 and are believed to be allowable therefor, as well as for the recitations

independently set forth therein.

Claim 72 recites at least, "phase generator means for implementing the plurality

of instructions on the bus as the predefined sequence of bus transactions". Any

combination of Gates and Carlsson does not teach or suggest the structure described in

the specification corresponding to the phase generator means. In particular, there is no

teaching or suggestion of a plurality of phase engines that each correspond to a phase of a

bus transaction, as shown in one example for a Pentium(R) Pro bus in application Figure

5. Accordingly, claim 72 is believed to be allowable. Claims 73-74 depend on claim 72

and are believed to be allowable therefor, as well as for the recitations independently set

forth therein.

Claim 85 recites at least, "capturing a response to the predetermined sequence of

bus transactions ctions". Any combination of Gates and Carlsson does not teach or

suggest these limitations. Accordingly, claim 85 is believed to be allowable. Claims 86-

89 depend on claim 85 and are believed to be allowable therefor, as well as for the

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recitations independently set forth therein.

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Conclusion

In view of the foregoing, it is believed that all claims now pending patentably

define the subject invention over the prior art of record and are in condition for

allowance. Applicants respectfully request that the rejections be withdrawn and the

claims be allowed at the earliest possible date.

Request For Telephone Interview

The Examiner is invited to call Brent E. Vecchia at (303) 740-1980 if there

remains any issue with allowance of the case.

Request For An Extension Of Time

The Applicants respectfully petition for an extension of time to respond to the

outstanding Office Action pursuant to 37 C.F.R. § 1.136(a) should one be necessary.

Please charge our Deposit Account No. 02-2666 to cover the necessary fee under 37

C.F.R. § 1.17 for such an extension.

Charge Our Deposit Account

Please charge any shortage to our Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Date: Oct. 30 2003

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